REMARKS

Claims 1, 2, and 4-68 are all the claims currently pending in this Application. Claims 38-68 are withdrawn.

Allowable Subject Matter

The Examiner indicates that claim 9 contains allowable subject matter and would be allowed if rewritten into independent form including the limitations of the claims from which it depends. Applicants respectfully request that the rewriting of claim 9 be held in abeyance at this time.

Rejections

Claims 1, 2, 4-8, 10-24, 31, and 34-37[1] are rejected under 35 U.S.C. § 102(e) as allegedly anticipated by Paton (U.S. Patent 6,703,277). Claims 25-29, 32, and 33 are rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Paton in view of Jeon (U.S. Patent 6,586,349). Claim 30 is rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Paton in view of Jeon and Green (U.S. Publication 2003/0219972). These rejections are maintained form the previous Office Action.

In the Rule 1.111 Response of January 7, 2009, Applicants submitted that none of the references, either alone or in combination, disclose or suggest the combination of layers recited in claim 1.

Namely, the references fail to disclose or suggest at least: an insulating film structure comprising: (a) "at least one silicon oxide region composed of a silicon oxide not containing said

[1] At page 2 of the Office Action, the Examiner lists claims 1, 2, 10-26, and 31-37 in this rejection. However, in the rejection itself, claims 1, 2, 4-8, 10-24, 31, and 34-37 are discussed.

at least one metal element"; (b) "at least one metal rich region having high concentration of said at least one metal element"; and (c) "at least one silicate region which is located between said silicon oxide region and said metal rich region and has a lower concentration of said at least one metal element that that of said metal rich region".

Regarding Paton, Applicants submitted that Paton is generally directed to a semiconductor device. Figures 2-5B illustrate the fabrication of a MOS structure. The first steps in the method of creating the device are shown in Figures 2-4A. A high-K dielectric material 108 is deposited on a silicon substrate 102. The deposition of the high-K layer 108 also results in the formation of an unwanted interfacial silicon dioxide layer 118 between the high-K dielectric layer 108 and the substrate 102. (col. 9, lines 33-37) The thickness of the interfacial silicon dioxide layer 118 varies, and in one embodiment, the process by which it is formed may be adjusted to minimize the formation of this layer 118. (col. 10, lines 49-59)

Thereafter, a metal layer 120 is formed on the high-K dielectric layer 108. Figure 3 illustrates the process after the metal layer 120 has been formed. (col. 10, lines 60-65). The metal layer 120 may comprise halfnium, which, during an oxidation-reduction reaction, may react with silicon dioxide for form halfnium silicate. (col. 11, lines 10-21).

After the metal layer 120 is formed, a gate layer 110 is deposited on the metal layer 120. (col. 11, lines 22-25).

Thereafter, the structure (including the substrate 102, the interfacial silicon dioxide layer 118, the high-K dielectric layer 109, the metal layer 120, and the gate electrode layer 110) is further processed by etching to form a gate stack as shown in Figure 4B.

Thus, according to one embodiment, shown in Figure 4B, the interfacial silicon dioxide layer 118 remains, and there has been no thermal processing for an oxidation-reduction reaction. The resultant layers between the silicon substrate and the gate 110 are: (1) the interfacial silicon dioxide layer 118, (2) the high-K dielectric layer 108, and (3) the metal layer 120. There is no silicate layer.

According to another embodiment, prior to processing and etching to form the gate stack(or possibly after: col. 12, lines 3-9), the structure of Figure 4A is subjected to thermal processing. (col. 11, lines 63-67) In this embodiment, as a result of thermal processing, the metal layer 118, which may be halfnium, as discussed above, diffuses through the high-K dielectric layer 108 to reach the interfacial silicon dioxide layer. At the appropriate temperature, there is an oxidation-reduction reaction between the metal and the silicon dioxide. Thus, the silicon dioxide layer "is converted to a metal oxide layer 116". (col. 12, lines 9-27) The metal oxide layer may contain some amount of silicon. (col. 12, lines 24-26) As noted above, if the metal is one such as halfnium which forms a silicate, in the oxidation-reduction reaction, the metal (e.g. halfnium oxide) reacts with the silicon dioxide to form a silicate (e.g. halfnium silicate). (col. 11, lines 15-21).

**Thus, according to this alternate embodiment, the metal layer 120 diffuses through the high-K dielectric layer 108 and reacts with the silicon dioxide layer 118 to change the silicon dioxide layer into a metal oxide layer 116 *or* to change the silicon dioxide layer into a silicate layer. The resultant layers between the silicon substrate and the gate 110 are: (1) a layer of metal oxide 116 *or* a layer of silicate, and (2) the high-K dielectric layer 108. While the metal oxide

may contain some amount of silicon, there is no silicon oxide layer *having no metal* and there is *no metal-rich layer.***

In the "Response to Arguments" of the current Office Action, the Examiner asserts that the claimed combination of layers (a metal-rich layer, a silicate layer having some metal element, *and* a silicon dioxide layer having *no* metal element) is disclosed by Paton. The Examiner asserts that the metal layer of Paton reacts with the silicon dioxide to form a silicate having less metal than the metal layer. This is true according to the second embodiment described above. The Examiner then asserts that as the thermal process is optional, in another embodiment, the interfacial silicon dioxide layer 118 may remain. This is also true according to the first embodiment described above. The Examiner then asserts that this means that claim 1 is anticipated by Paton. Applicants respectfully disagree.

According to Patton, in one embodiment, there is no thermal processing, and the interfacial silicon dioxide layer remains. *The result is a gate stack including a silicon dioxide layer 118 and a metal layer 120, but no silicate layer including metal.* According to a different embodiment, there is thermal processing, and the metal layer 120 may react with the silicon dioxide layer 118 to form a silicate including metal. *The result is a gate stack including a silicate layer including metal, but no metal rich layer and no silicon oxide layer having no metal.*

In the "Response to Arguments," the Examiner appears to combine these two different embodiments to achieve the combination of layers recited in claim 1. However, this is not possible. According to Paton, in order to form the silicate layer, the metal layer and the silicon dioxide layer react to form the silicate layer. First, there is no disclosure of any way to *maintain* the metal layer 120 *and* the silicon dioxide layer 118 *and* also create the silicate layer. Second,

Paton specifically describes that the silicon dioxide layer is *unwanted*. In the Paton device, sicne the thickness of the silicon dioxide layer 118 is at most 10Å as described in col, 10, lines 54-57, the silicon dioxide layer 118 is entirely removed when it reacts to form the silicate layer. This is why, in the second embodiment discussed above, the silicon dioxide layer is removed by combining it with the metal layer to form the silicate. Not only does Paton fail to disclose or suggest any way of maintaining the silicon dioxide layer and the metal layer *in addition* to the silicate layer, *it is specifically undesired*.

Therefore, Applicants submit that Paton fails to disclose or suggest the combination of layers as recited in claim 1. Applicants further submit that neither Jeon nor Green makes up for the above-discussed deficiencies of Paton.

Applicants submit that claim 1 is patentable over the cited references and that claims 2, 4-8, and 10-37 are patentable at least by virtue of their dependencies. Applicants respectfully request that the rejections be reconsidered and withdrawn.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

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